



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENT AND TRADEMARK OFFICE  
Washington, D.C. 20530  
WWW.USPTO.GOV

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,610	11/28/2001	Kunihiko Kawabata	100353-00086	9276

7590 12/19/2002  
ARENT FOX KINTNER PLOTKIN & KAHN, PLLC  
1050 Connecticut Avenue, N.W., Suite 600  
Washington, DC 20036-5339

EXAMINER

PHAM, LY D

ART UNIT PAPER NUMBER

2878

DATE MAILED: 12/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/994 610

Applicant(s)

KAWABATA ET AL

Examiner

Ly D Pham

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on 30 September 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☐ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 7-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on 20 November 2001 is/are a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

### Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Election/Restrictions*

2. Applicant's election without traverse of claims 1 – 6 in Paper No. 4 is acknowledged.

Claims 7 – 20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention(s), there being no allowable generic or linking claim.

Election was made **without** traverse in Paper No. 4.

3. Claims 1 – 6 are presented for the examination.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1 – 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furutani et al. (US Pat 5,305,261) in view of Padgett (US Pat 5,079,332).

Regarding **claim 1**, Furutani et al. disclose a semiconductor device comprising:

signal lines over which signals are transferred (fig. 1, lines connecting equalize/precharge 2 to memory cell array 3, col. 17, lines 18 – 20); and

a driver circuit driving the signal lines in operating modes (fig. 1, input/output circuit 6).

Although Furutani et al. did not disclose the operating modes including a dynamic operation mode in which the signal lines are precharged, and a static operation mode in which the signal lines are not precharged, the mentioned features are shown by Padgett (col. 1, lines 15 – 19 illustrate a dynamic operation mode requiring precharge circuits, and col. 1, lines 45 – 50 show a static operation mode requiring no precharge circuit).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to incorporate the features disclosed by Padgett to the invention of Furutani so that various operation modes in a semiconductor device can be implemented to improve application versatility.

Regarding **claim 2**, Furutani further discloses a memory cell array (fig. 1, memory cell array 3) to which the signal lines are connected (signal lines IO in fig. 10), data read from the memory cell array being transferred over the signal lines (fig. 10, test data input 922 transferred over the signal lines).

Regarding **claim 3**, Furutani also discloses a test-dedicated line (col. 5, lines 10 – 12), a predetermined test of the semiconductor device being performed using the test-dedicated line and the signal lines (fig. 10, test data input 922 connect to signal lines).

Regarding **claim 4**, Furutani further discloses a circuit receiving the signal lines at inputs thereof and outputting a test result (fig. 10, line test circuit 5 outputs test result, shown error in figure), said test result and a logic level of the test-dedicated line forming a result of the

Art Unit: 2818

predetermined test (dedicated test data line being wired-ANDed implies that its test output has to be a certain logical state).

Regarding **claim 5**, Furutani further discloses a precharge circuit precharging the signal lines and the test-dedicated line (abstract: the semiconductor memory device further includes a load circuit which precharges the internal data transmitting lines to a predetermined potential in a test mode, and a line test circuit which determines existence and nonexistence of a defective memory cell based on the potentials of the internal data transmitting lines).

Regarding **claim 6**, as disclosed by Padgett, col. 1, lines 15 – 17, only dynamic operation mode requires the precharge circuit, therefore, the precharge circuit precharges the signal lines and the test-dedicated line in the dynamic operation mode only.

### *Conclusion*

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. When responding to the office action, Applicant(s) are advised to provide the examiner with the page and line numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

7. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

Art Unit 2818


8. Any inquiry concerning this communication on earlier communications from the examiner should be directed to Ly Pham, whose telephone number is 703-305-4862. The examiner can normally be reached on Monday – Friday from 8:30am to 5:00pm, alternate Friday off. The examiner's supervisor, David Nelms, can be reached at 703-308-4910. The fax number for the organization where this application or proceeding is assigned is 703-308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Ly Pham



December 11, 2002

  
HOANG  
PRIMARY EXAMINER